REMARKS

The outstanding Action has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Prior to this Amendment, claims 1-12 are pending in this application of which claims 10-12 have been withdrawn from consideration. By this Amendment, claims 1-3, 5-6 and 8-9 have been cancelled without prejudice or disclaimer, and claims 4 and 7 have been amended and claims 13-16 have been added to further set forth the invention. No new matter has been added. Accordingly, claims 4, 7 and 13-16 are now submitted for consideration.

Drawing Objection

The drawings are objected to due to certain informalities

Attached is a Request for Approval of Drawing Correction with a proposed change to Fig. 1 in red ink. Upon approval of the Request, a formal drawing thereto will be timely filed. The Applicants respectfully request that the objection be withdrawn.

Claim Rejections

Claims 1-3 are rejected under 35 U.S.C. §102(b) as being anticipated by Tanaka (U.S. Patent No. 6,011,720, hereinafter "*Tanaka*").

This rejection is now moot in view of the cancellation to claims 1-3.

Claim 4 is rejected under 35 U.S.C. §103 as being unpatentable over *Tanaka* in view of Takeuchi et al. (U.S. Patent No. 5,986,933, hereinafter "*Takeuchi*").

Claim 4 has been properly rewritten in independent form and amended to further clarify that the unit of erasure includes more than one but not all of the input/output terminals.

By contrast, ***Tanaka*** merely selects one word line, and applies a positive potential to the selected word line, with a negative potential being applied to a plurality of source nodes or the substrate, so as to ensure erasure by the unit of one word line. As a result, data of all the input/output terminals are erased at once with respect to the selected word line by the unit of erasure.

On the other hand, the erasure in ***Takeuchi*** is performed for each of sub-cell arrays or for two sub-sell arrays (see 9: 56-58). Alternatively, the erasure is performed for each block of each sub-cell array or for blocks of a plurality of sub-cell arrays (see 10: 30-35). Therefore, the sub-cell array and block each includes all the I/Os (see 12: 57-60 and 11: 17-22).

As such, neither ***Tanaka*** nor ***Takeuchi***, individually or in combination thereof, teaches erasing data of more than one but not all of the input/output terminals as now set forth in claim 4 (and also claims 7 and 13-16). Instead, both ***Tanaka*** and ***Takeuchi*** teach erasing data of all the input/output terminals by the unit or erasure (i.e., at once).

Claims 5-9 are rejected under 35 U.S.C. §102(b) as being anticipated by Takeuchi et al. (U.S. Patent No. 5,986,933, hereinafter "*Takeuchi*").

The rejection with respect to claims 5, 6, 8 and 9 are not moot in view of the cancellation thereto.

Claim 7 has also been properly rewritten in independent form and amended to further clarify that the unit of erasure includes more than one but not all of the input/output terminals. Therefore, claim 7 is also patentable over ***Tanaka*** for at least the reasons stated above.

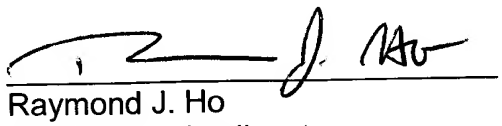
In view of the above remarks, the Applicants respectfully submit that each of claims 4, 7 and 13-16 recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicants submit that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. Applicants therefore request that each of pending claims be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not timely filed, the Applicants respectfully petition for an appropriate extension of time.

Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,



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Enclosures: Marked-Up Copy of Amended Claims
Petition for Extension of Time

MARKED-UP COPY OF AMENDED CLAIMS

4. (Amended) [~~The~~] A semiconductor memory device [~~as claimed in claim 3~~], comprising :

a plurality of input/output terminals;

a memory cell array which are divided into blocks respectively corresponding to said input/output terminals such that only one of the blocks corresponds to a given one of said input/output terminals;

sense amplifiers, which are connected to the blocks at a side thereof, and amplify data of said memory cell array;

switches which are respectively connected to said sense amplifiers; and

signal lines, which connect said sense amplifiers to a corresponding one of said input/output terminals via the switches, wherein said memory cell array includes flash memory cells, wherein data of said memory cell array is erased by one unit of erasure, wherein more than one but not all of said blocks are put together to form the unit of erasure.

7. (Amended) [~~The~~] A semiconductor memory device [~~as claimed in claim 6,~~] which allows data of a plurality of pages to be read from a memory cell array and stored in sense amplifiers, and allows data of a selected page to be read from the sense amplifiers and output to an exterior of said semiconductor memory device, comprising:

memory cell areas storing data to be input from and output to one common input/output terminal, said memory cell areas respectively corresponding to the plurality

of pages and provided adjacent to each other, wherein the sense amplifiers corresponding to said memory cell areas are arranged adjacent to each other; and

signal lines which connect the sense amplifiers corresponding to said memory cell areas to the common input/output terminal, wherein the memory cell array includes flash memory cells, wherein data of said memory cell array is erased by one unit of erasure, wherein the unit of erasure is formed by putting together the memory cell areas for [a ~~plurality~~] more than one but not all of input/output terminals.